

PATENT APPLICATION

PULSED CURRENT GENERATOR CIRCUIT WITH CHARGE BOOSTER

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PULSED CURRENT GENERATOR CIRCUIT WITH CHARGE BOOSTER

FIELD OF THE INVENTION

[0001] This invention relates generally to circuitry for testing electrical components and circuits, and more particularly the invention relates to current pulse circuitry for use in such testing.

BACKGROUND OF THE INVENTION

[0002] Current pulses are often employed in testing electrical components and circuits. When high repetition rate current pulses are required, for example with pulsed electromigration tests, the desired pulse waveform is usually rectangular. Therefore, the transitions between current levels must be abrupt with minimal overshoot to effectively provide the intended current drive at each level. See Fig. 1 for bipolar and unipolar current pulses, respectively. Ideally, the transition from ground level ("0") to the required current ("Ap" or "An", or generally "A" for simplicity) is abrupt, as shown in Fig. 1. In reality, however, such transitions take time and can be too slow to reach the required maximum level A.

[0003] An effective technique to achieve current pulses is implemented by connecting a constant (DC) current source to ground and thereby shunting the current from a device under test (DUT) as shown in Fig. 2. Here, current flow through the device under test (DUT) is shunted to ground by shunt transistor, Qs, in response to a control signal at point P which is connected through resistor Rx to shunt transistor Qs. The desired waveform is achieved in response to the timing generator having a required period T, "on" time t and "off" time (T-t). See for example Krieger et al. U.S. Patent No. 6,249,137 for CIRCUIT AND METHOD FOR PULSED RELIABILITY TESTING.

[0004] In general, it is relatively easy to generate an ideal driving pulse at the gate of the main shunting transistor Qs (point "P" in Fig. 2). Similarly, modern power transistors can provide both very low on resistance and very fast intrinsic transition between their on and off states in both directions. A problem is the parasitic capacitance Co between the output node "C" and Ground (Gnd), which includes the output capacitance of Qs, any stray capacitance associated with the DUT, the output capacitance of the DC current source and any other

capacitance introduced by the test setup, such as cables or test fixtures. Reducing this capacitance to a desirable level is difficult, since it is strongly related to I_{dc} and to the current sinking capability of Q_s . With pulsed current applications often requiring wide range of current levels, it is impractical to sacrifice high-current characteristics in favor of low-current performance and vice versa. In fact, the problem is limited to low and perhaps medium currents; however, to assure proper high current operation both Q_s and the DC current source must be sufficiently strong, implying large values of C_o accordingly.

[0005] This limitation is not an issue when voltage pulses, rather than current, are involved. Most voltage sources are capable of driving relatively large currents while trying to reach the intended level (A or Ground, depending on the specific transition); therefore inherently generating fast transitions. In the pulsed current source case, I_{dc} is simply diverted to Q_s while it is on, as C_o discharges through Q_s simultaneously. While Q_s is off, C_o is charged exponentially to the steady state level $V_o = (R_{dut})(I_{dc})$, with a time constant $\tau = (C_o)(R_{dut})$. As low current applications often require R_{dut} of several kilo-ohms ($k\Omega$) and C_o is rarely less than 20 pF, the resulting time constant is several tens of nanoseconds. On the other hand, since R_{on} is very small, C_o discharges very quickly after Q_s enters its on state; thus posing no practical delay.

[0006] The present invention is directed to facilitating fast current transition from 0 to A through DUT with transition time, t_r , substantially shorter than the related pulse duration, t_p , t_n , and with an acceptable minimal overshoot.

SUMMARY OF THE INVENTION

[0007] In accordance with the invention, a charge boost circuit is provided to facilitate the rapid recharge of parasitic capacitance associated with a DUT when current is re-applied through the DUT. Short bursts of current are provided during the transitions of the shunt transistor from on state to off state, with the magnitude of the charging current being greater than the magnitude of the pulsed current. A current limiter prevents overcharging of the parasitic capacitance thereby avoiding unacceptable overshooting in the resulting current pulse waveform.

[0008] The invention and objects and features thereof will be more readily apparent from the following detailed description and appended claims when taken with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

- [0009] Fig. 1 illustrates bipolar and unipolar current pulses for use in testing electronic devices.
- [0010] Fig. 2 illustrates a conventional pulse current generator for a DUT.
- [0011] Fig. 3 illustrates a pulsed current generator in accordance with the invention.
- [0012] Fig. 4 illustrates one embodiment of a pulse generator and charge booster circuit in accordance with the invention.
- [0013] Fig. 5 illustrates another embodiment of a pulse generator and charge booster circuit in accordance with the invention.
- [0014] Fig. 6 illustrates another embodiment of a charge booster circuit in accordance with the invention.
- [0015] Fig. 7 illustrates waveforms in the circuit of Fig. 5 with proper setting and improper setting, respectively, for charge boosting.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

- [0016] Fig. 3 corresponds to the circuit of Fig. 2 with a booster circuit 10 in accordance with the invention for providing short bursts of current during the transitions from the on to off state of shunt transistor Q_s . During this transition period, booster circuit 10 provides current through switch S1 which facilitates the charging of parasitic capacitor C_o . Since the booster current is much higher than the current I_{dc} from the current source, recharging of the parasitic capacitor is facilitated. Booster circuit 10 and switch S1 respond to control circuitry 12 and the control voltage at node P for shunt transistor Q_s .
- [0017] Fig. 4 is a schematic of one embodiment of the pulsed current generator of Fig. 3 which further illustrates booster circuit 10 and control circuit 12. Here the timing generator at terminal P is connected to the gate of the main shunt transistor Q_s via two serially connected buffers 20, 22 with each buffer inverting its input signal while adding a small delay (t_d). The resulting waveforms at P1, P2 and timing generator signal at P are all shown in the figure. Note that the coupling gate resistor R_x is not critical and is commonly added just to avoid direct coupling between the transistor gate and the driving signal.

[0018] The rest of the circuit forms the booster shown at 10. The path of the current injected by the booster into the output node C comprises NMOS transistor Q_n and PMOS transistor Q_p, capacitor C_{ba} and resistor R_y. As booster activation/deactivation is done electronically, the role of switch S1 is just to eliminate any parasitic coupling through stray capacitance and leakage. Resistor R_y sets an upper bound to the boosting current to avoid overheating and large overshoots. Capacitor C_{ba} is sufficiently large (about one μF or more) to assure constant (DC) voltage at the common source node S, even when strong boosting action is required.

[0019] Proper operation of the booster is based on an unambiguous knowledge of the actual conditions at node C in real time and comparing to an intended target. The target is simply a resulting “high” voltage level at node C being the same as the resulting voltage level under similar DC operation. In other words, before the intended timing generator is applied, I_{dc} is set to the required level and the resulting voltage at node C is measured and acquired. Next, the timing generator is activated and the resulting voltage at C is measured, using a peak detector which acquires the highest level of the measured waveform (peak detector not shown). As the whole idea is to have I_{dc} flowing into the DUT while the main shunting transistor Q_s is off, this peak, being exactly the same as observed under similar DC conditions, assures proper operation. Measuring lower or higher level will turn the boosting action up or down, respectively, in an iterative algorithm which assures proper convergence after a few such steps.

[0020] To implement the above, the voltage levels at Y1 and X1 must be set appropriately based on the related data from the peak detector at node C. First and foremost, no DC current can flow through Q_p, meaning that as long as the timing signal at P is not applied either Q_p or Q_n is off. This requirement is satisfied by the following relation:

$$V_{X1} - V_{Y1} > V_{tp} - V_{tn}$$

where V_{tn} is positive for enhancement devices and negative for depletion, while V_{tp} is negative for enhancement and positive for depletion. In particular, when a combination of depletion NMOS transistor (Q_n) and enhancement PMOS transistor (Q_p) is selected and assuming that their absolute values are about the same (i.e. $|V_{tn}| \approx |V_{tp}|$), setting V_{X1} slightly higher than V_{Y1} assures no DC current flow through Q_p. In reality, an extra “safety margin” of a few tenths of a volt may be added as part of circuit adjustment during production. Once

the optimal difference $V_{X1} - V_{Y1}$ is known, the system must keep it for each and every level. In this respect, the implementation shown in Fig. 4 is unnecessarily cumbersome as it requires two independent adjustable voltage sources, while only one of them is varied by the internal algorithm, as the other is at constant distance from it (i.e. $V_{X1} = V_{Y1} + \Delta$, where Δ is the pre-adjusted constant described above). Two other embodiments, where the above is achieved with one adjustable voltage source and another fixed source, are shown in Figs. 5 and 6, respectively. Similar to capacitor C_{ba} , capacitors C_{bb} and C_{bc} are sufficiently large to assure DC conditions at $Y1$ and at $X1$, respectively. Resistors R_d are added to avoid loading the operational amplifiers with large capacitance. As point Y is connected only to the gate of Q_n , where only negligible leakage current flows, V_Y is practically equal to V_{Y1} and resistor R_e is not very significant. The situation is different at the gate of Q_p (point X), where under pulsed operation the waveform differs significantly from V_{X1} and the specific values of R_f , C_t and even the intrinsic PMOS input capacitance C_{ip} are important.

[0021] In Fig. 5, V_b can be any available low voltage power supply (e.g. +5 V), while the variable resistor R_p allows pre-setting of V_{Y1} within a desirable range above and below V_{X1} , according to the following relations:

$$V_{X1} = V_b (R_c/R_a) - V_{bst} (R_c/R_b) \quad (V_{bst} \equiv \text{Variable Source})$$

$$V_{Y1} = V_b [R_c/(R_a - \delta + R_p)] - V_{bst} (R_c/R_b) \quad (\delta < R_{pmax} < R_a)$$

Which implies:

$$V_{X1} - V_{Y1} = V_b [R_c (R_p - \delta)] / [R_a (R_a - \delta + R_p)] \equiv \Delta$$

[0022] By adjusting R_p between 0 and R_{pmax} , the necessary value of $(V_{X1} - V_{Y1})$ is obtained. Similarly, another embodiment of $V_{X1} - V_{Y1} = \Delta$ is shown in Fig. 6, as an alternative to section 50 on the top left of Fig. 5. Here V_{Y1} is V_{bst} , the variable voltage source, while any combination of two available fixed sources provides the required difference Δ . By using fixed voltage sources with the same magnitude and opposite polarity (for example, +5 and -5 Volt), the difference can vary between $-|V_b| R_p/(2R_y + R_p)$ and $+|V_b| R_p/(2R_y + R_p)$, according to the position of the center terminal of R_p .

[0023] Pre-setting the required value of Δ which assures no DC current flow through Q_p , the actual boosting can take place. This is achieved by the switching action of transistor Q_d , the coupling capacitor C_t , resistor R_t and resistor R_f , as follows: When the inverted timing generator pulse at point P rises from low (Gnd) to high, Q_d turns abruptly into a

powerful current sink, driving its drain node to near ground level. The transient abruptly propagates to the gate of Qp (point X), driving it sharply lower (the exact drop is a fairly complex function of the various components involved). At this point, the short inverter delay t_d is over and the main shunt Qs, whose gate is driven by the signal at point P2, is turned off, as the signal at P2 drops to Gnd level. With Qp strongly on, a surge of boosting current flows into Co and the DUT, quickly charging node C. Meanwhile, node X rises towards the level V_{X1} in a rate defined by Ct, Cip (the input capacitance of Qp), Rt and Rf, until Qp enters its off state again. The total time from the point Qd turns on and until Qp turns off again must be less than the minimum duration Qd is on, namely (T-t), for all applications and pulse repetition rates supported by the system. In principle, this timing mechanism could be used for terminating the boosting action; however, to assure the adequate boosting to achieve the required level at point C, with no excessive overshoot, an additional mechanism is used. Since $|V_{ds}| > 0$ is necessary for boosting current to flow, setting the voltage at S to about the same level of Vdut (point C) under DC condition (I_{dc} only) will do it properly.

[0024] Having the algorithm properly set, once the high level at C reaches its desirable value (the same level reached when I_{dc} flows under DC conditions) Qp will no longer drive boosting current, as its $V_{ds} \Rightarrow 0$. Shortly after, the voltage at its gate will reach off conditions, to be followed by the waveform at P1 turning to ground potential again. This will immediately turn Qd off, forcing the current from Va through Rt to charge Ct further, causing point X to rise above V_{X1} ; thus reversing the current direction through Rf. This change of direction, while not directly related to the actual boosting action, is nevertheless effective in restoring the charge Capacitor Cbc loses during the preceding action. This charging, controlled by the values of Rt and Rf, is important, as operational amplifier A has limited current drive. Furthermore, the related timing can be shortened as necessary by placing diode D1 across Rf, as shown in Fig. 5 (dashed lines). This charging action continues until the voltage at X reaches a slight peak and then starts to gradually converge toward V_{X1} , as the drain of Qd charges up and the charging current through Rt diminishes. The next transition marks the start of another pulsing cycle and so forth.

[0025] Essential to the above is a proper algorithm, controlled by a real-time computer and fed by the relevant data measured. The first step is setting up I_{dc} to the proper level with switch S1 open, no timing generator applied at P and with Vbst set to a level resulting in $V_{X1} \Rightarrow 0$, or even slightly negative if necessary. The voltage at point C is then acquired from the peak detector and stored as reference (hereunder " V_{cdc} "). Since V_{X1} (and V_{Y1} respectively)

are low enough to prevent boosting current, engaging S1 and applying the timing generator at P will turn Qs and Qd on and off accordingly with no boosting current through Qp. Next, the peak detector reading (V_{cp}) is acquired and compared to V_{dc} . If $V_{cp} > V_{dc}$ (very unlikely) then S1 should be disengaged. In the more likely case of $V_{cp} < V_{dc}$ boosting is needed. To initiate boosting, V_{bst} is increased until the resulting V_{cp} exceeds V_{dc} . At this point, V_{cp} is decreased and the process is repeated in a converging manner to the point where any further change has negligible effect. From here on, the required pulsing action is in effect. For sufficiently long pulses, the voltage at point C will gradually “converge” to the required level V_{dc} even without boosting; however, as the related time constant is significantly longer than short pulses (typically for $t < 500$ nS), such “convergence” provides little help and efficient boosting is necessary. Note that the actual algorithm used for the above iterations is not related to the invention, as it is a matter of efficient convergence. In reality, binary search or similar approaches are effective, but the invention is not limited to one particular algorithm or another and should be held as valid with any iterative algorithm used.

[0026] The waveforms in Fig. 7 provide more details as to the waveforms at points P1, P2, X and C (refer to Fig. 5). The left hand side shows proper setting of $\Delta (V_{x1} - V_{y1})$, leading to the expected output waveform. The right hand side shows insufficient boosting and the resulting improper output waveform due to excessive magnitude of Δ .

[0027] While the invention has been described with reference to specific embodiments, the description is illustrative of the invention and is not to be construed as limiting the invention. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention as defined by the appended claims.